An InGaSb p-Channel FinFET

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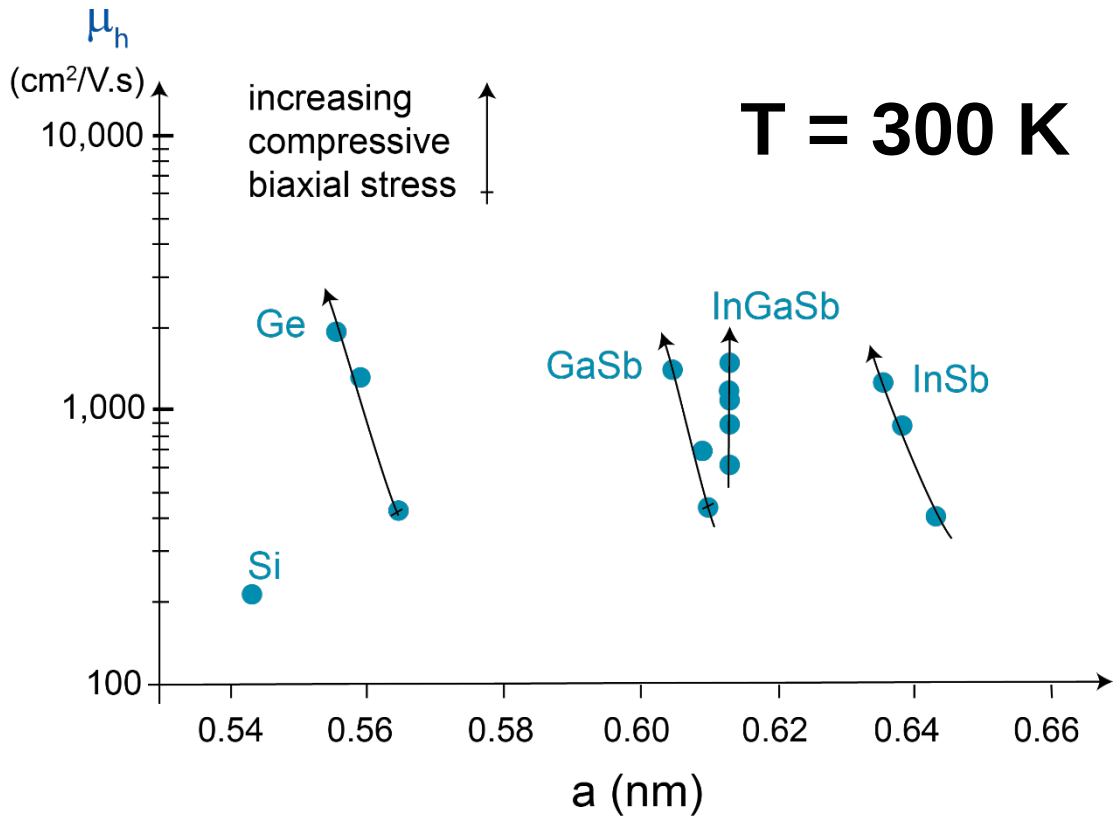
Sponsors: Samsung, Lam Research, DTRA

Motivation

From del Alamo, *Nature*, 2011

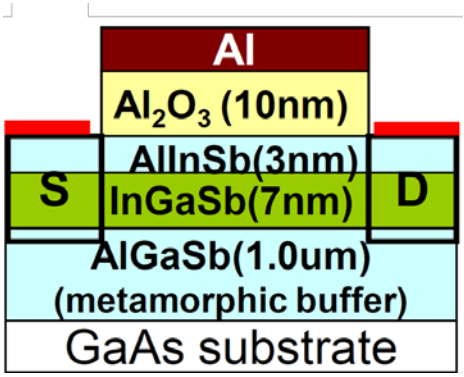


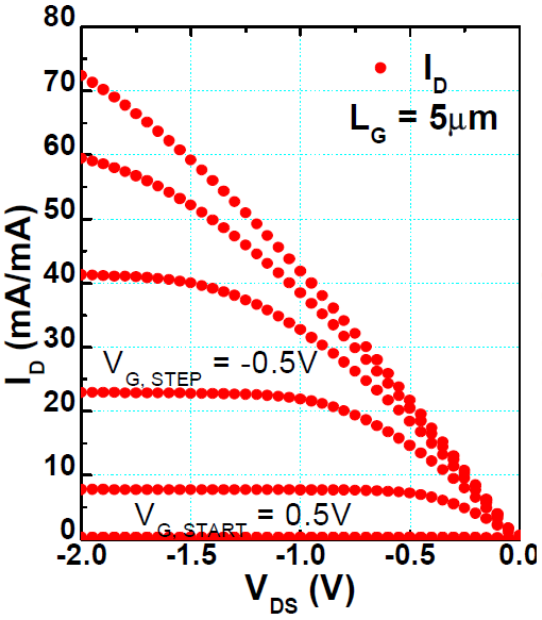
InGaSb as p-channel material for future III-V CMOS

Motivation

InGaSb p-MOSFET

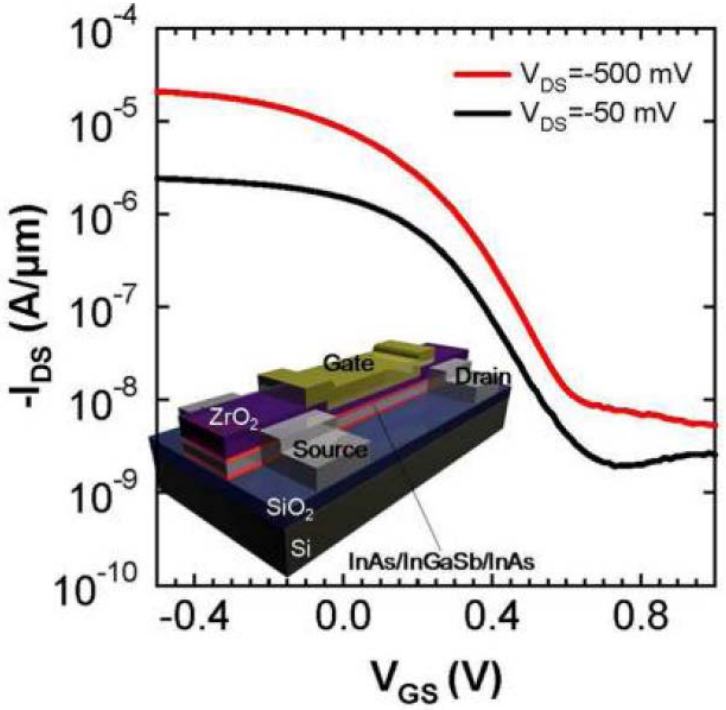
Nainani, *IEDM*, 2010





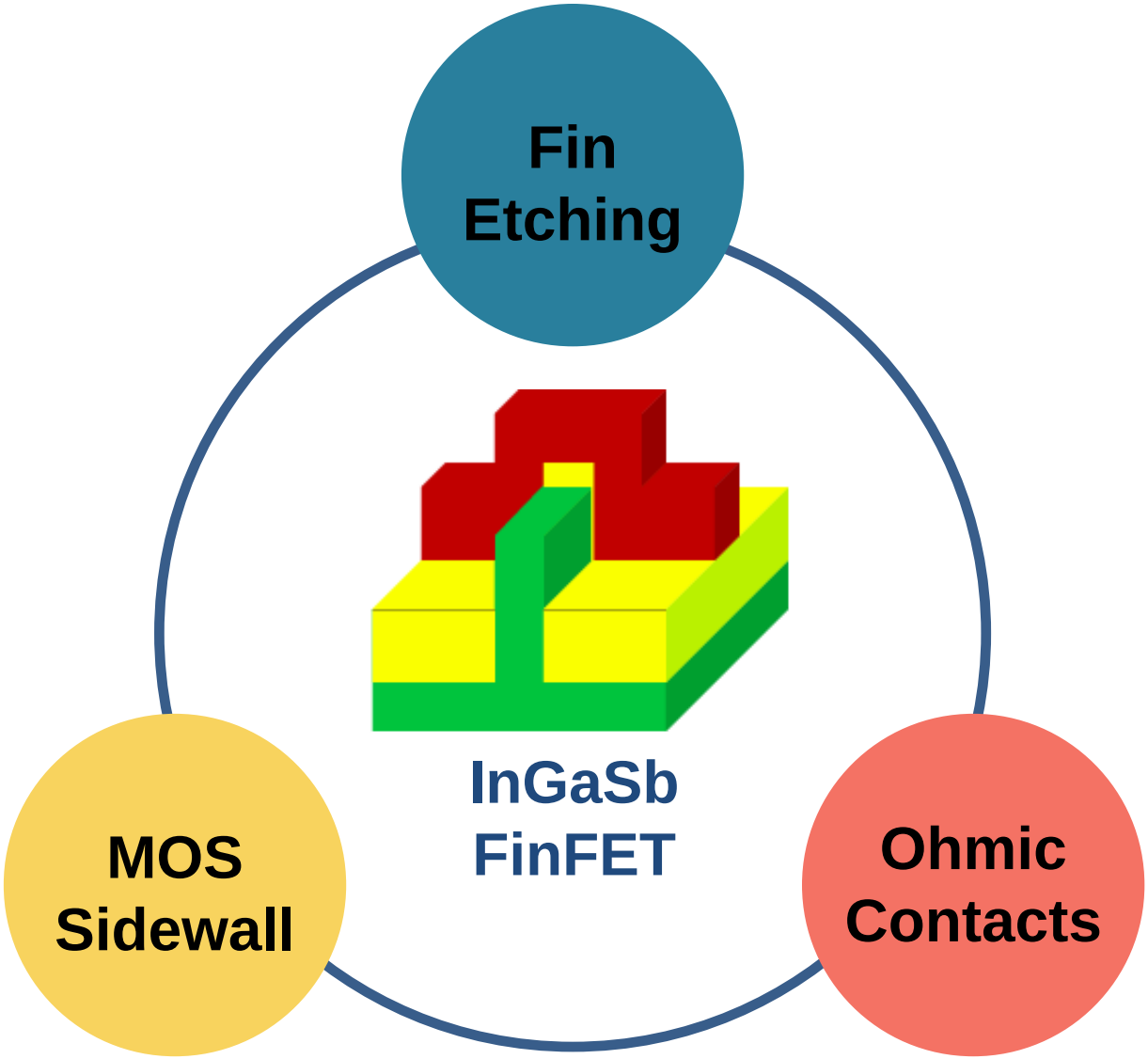
InGaSb XOI p-MOSFET

Takei, *Nano Lett.*, 2012



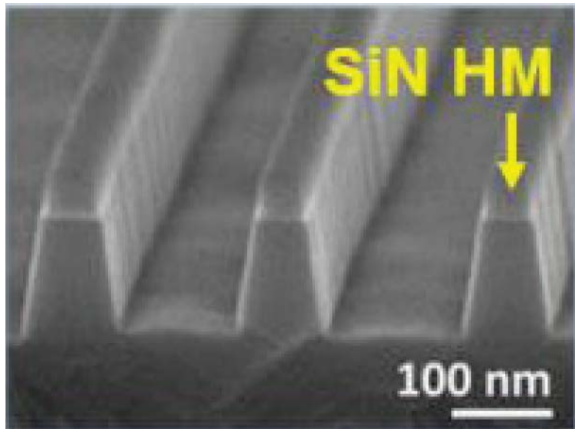
InGaSb multi-gate MOSFET needs attention!

Towards an InGaSb FinFET

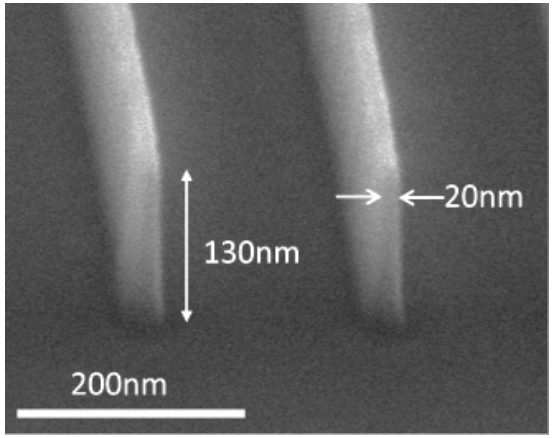


InGaAs Fin Etching

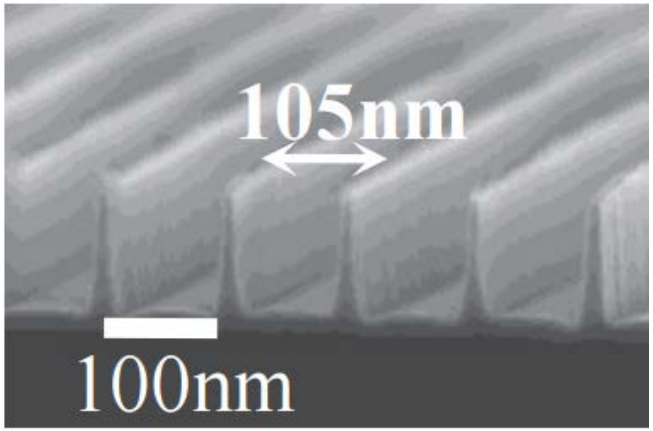
Rinus, *IEDM*, 2014



Vardi, *IEDM*, 2015



Thathachary, *VLSI*, 2015

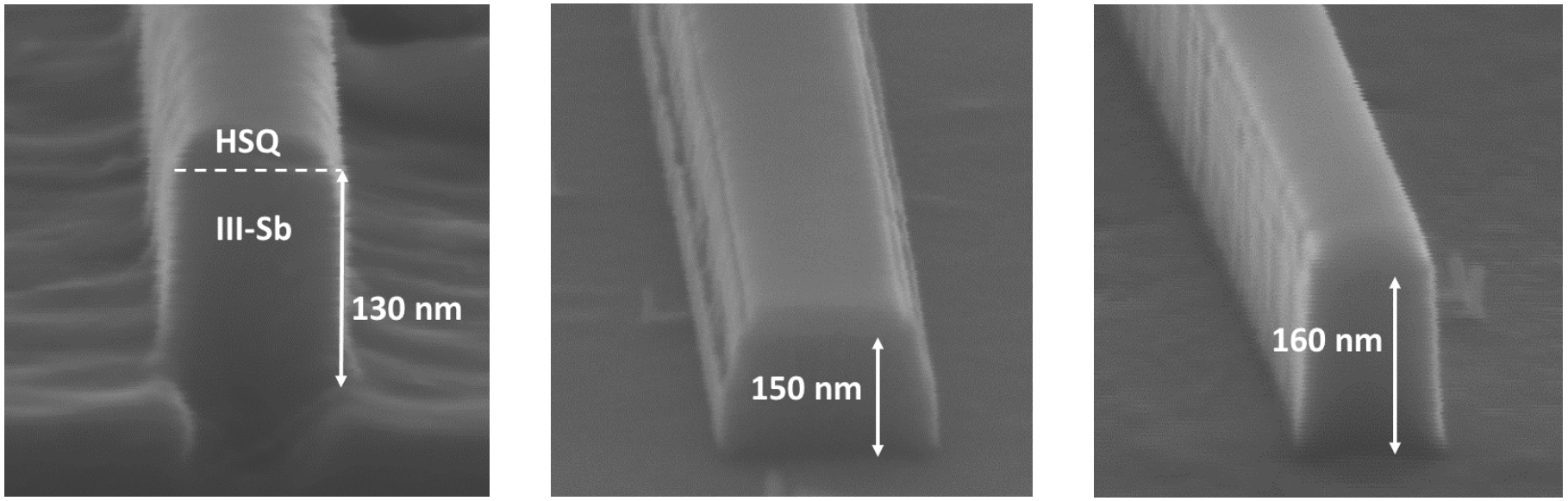


Excellent RIE enables InGaAs n-FinFETs

InGaSb Fin Etching

- **RIE by BCl_3/N_2 chemistry**

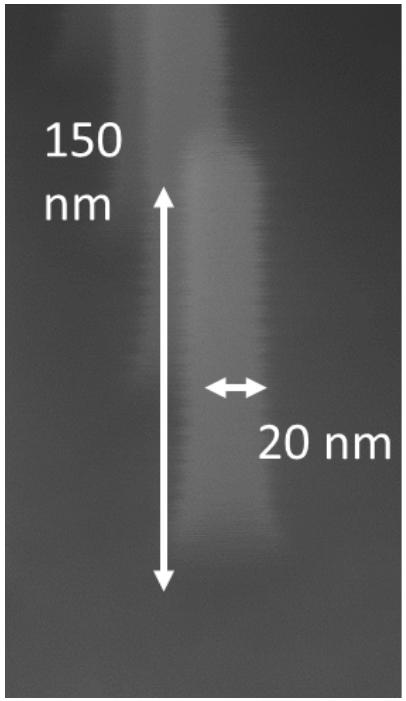
40 °C **120 °C** **250 °C**

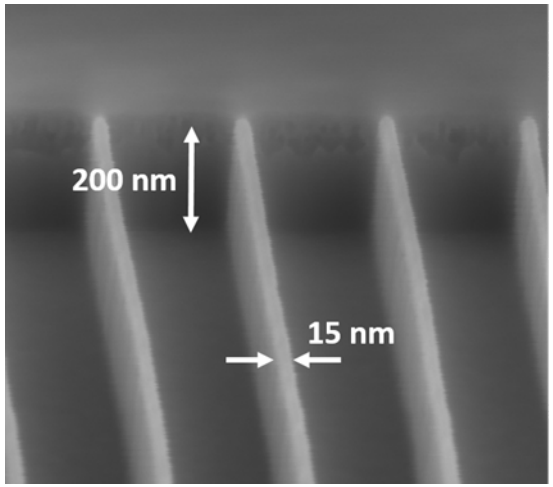


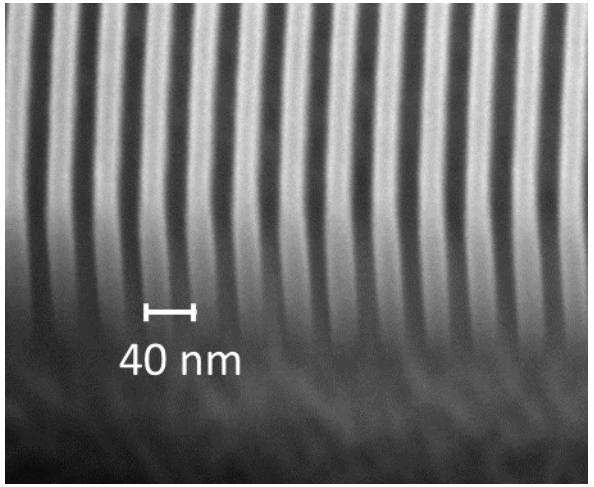
T ↑ → etch rate ↑, smooth surface, vertical profile

InGaSb Fin Etching

- **RIE by BCl_3/N_2 chemistry**



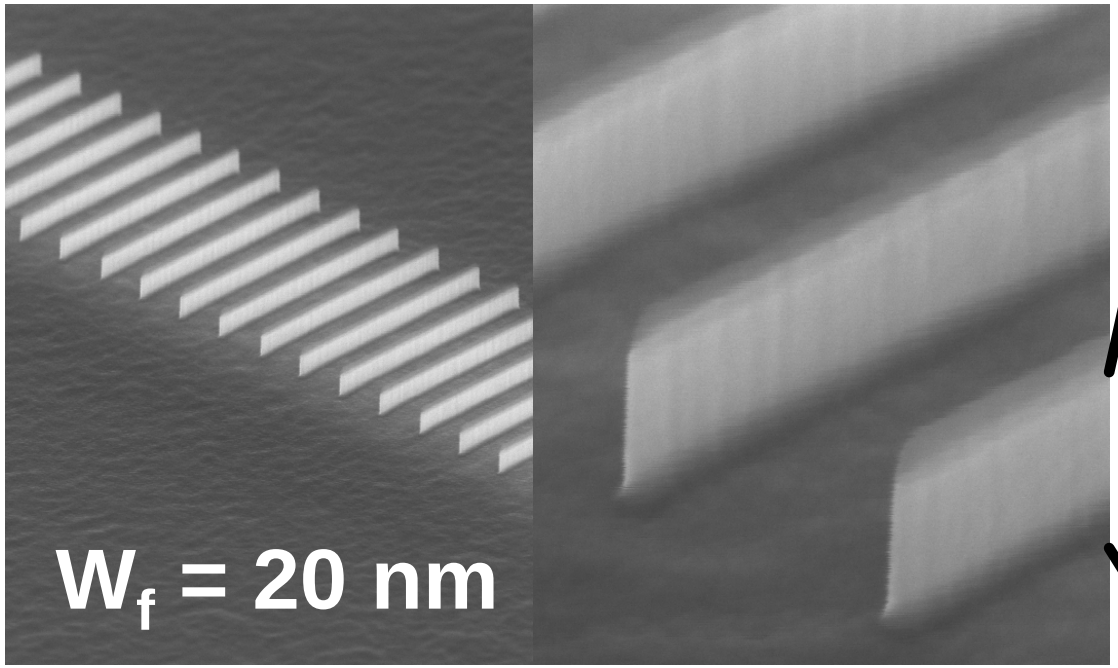


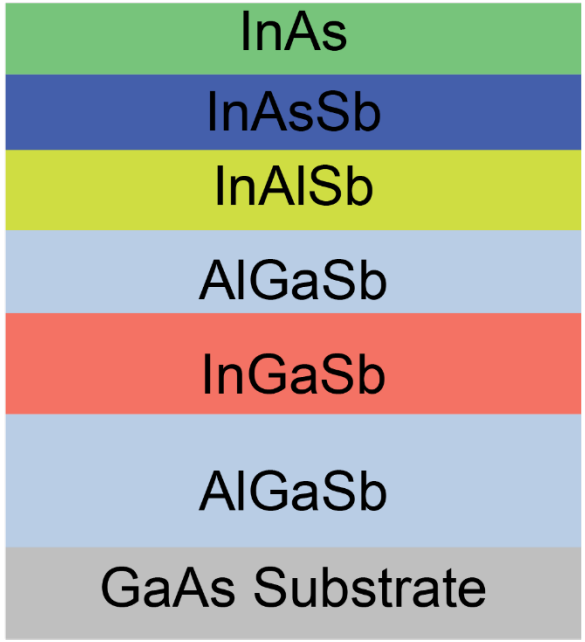


- Smallest W_f = 15 nm
- Aspect ratio >10
- Fin angle > 85°
- Dense fin patterns

InGaSb Fin Etching

- **RIE by BCl_3/N_2 chemistry**

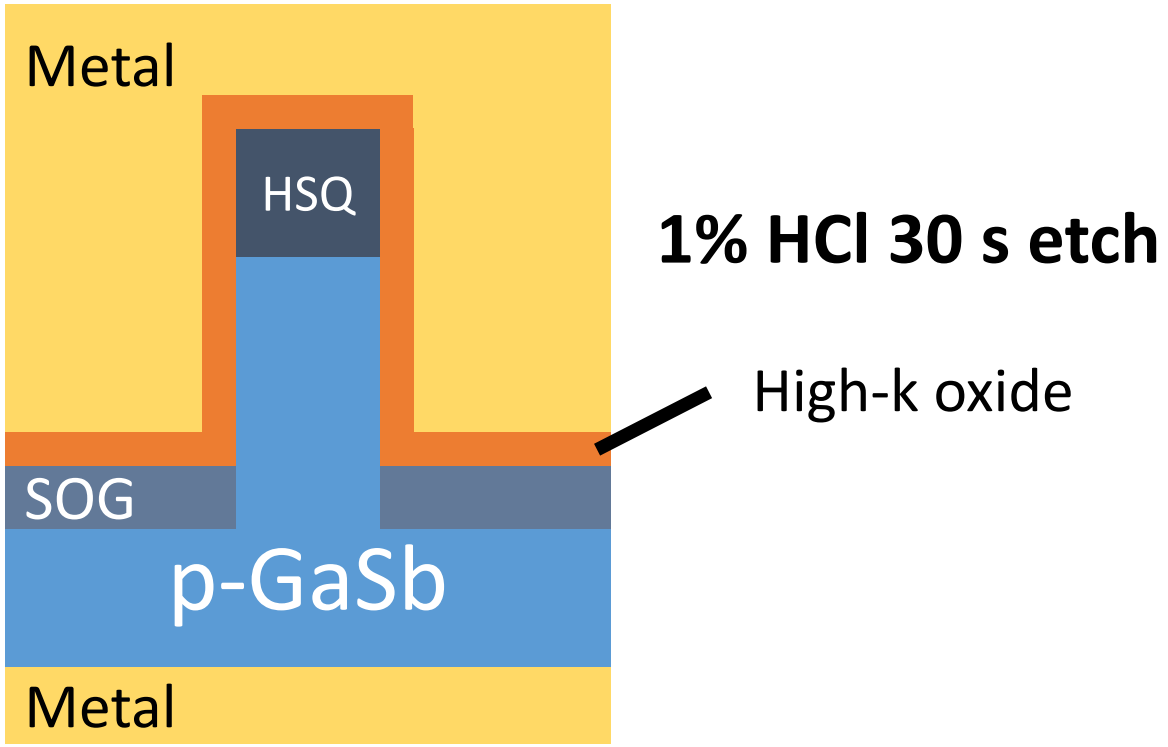




Smooth sidewall with no material selectivity

MOS Sidewall

- **How to characterize electrical quality of fin sidewalls?**

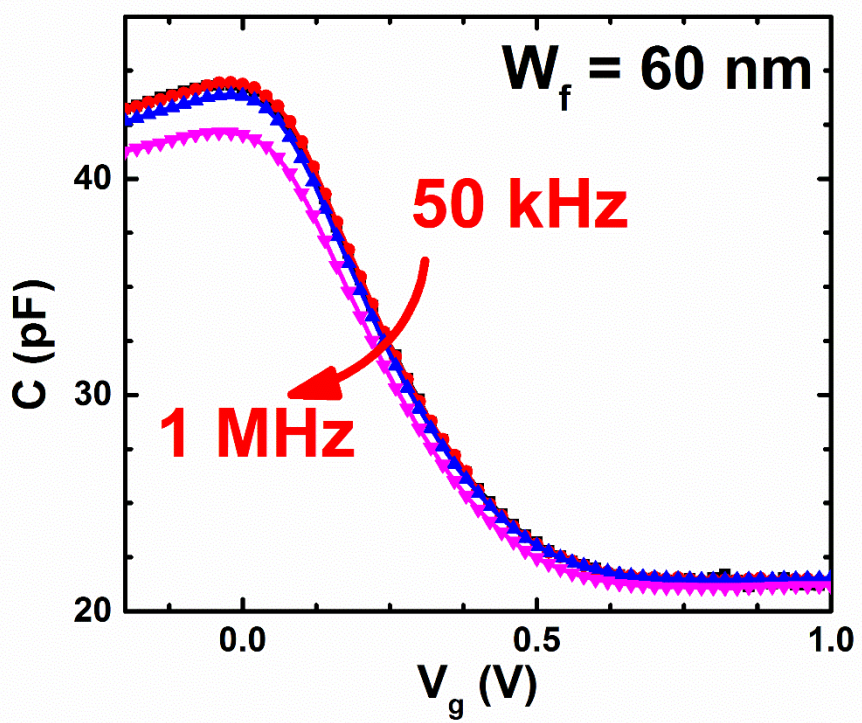


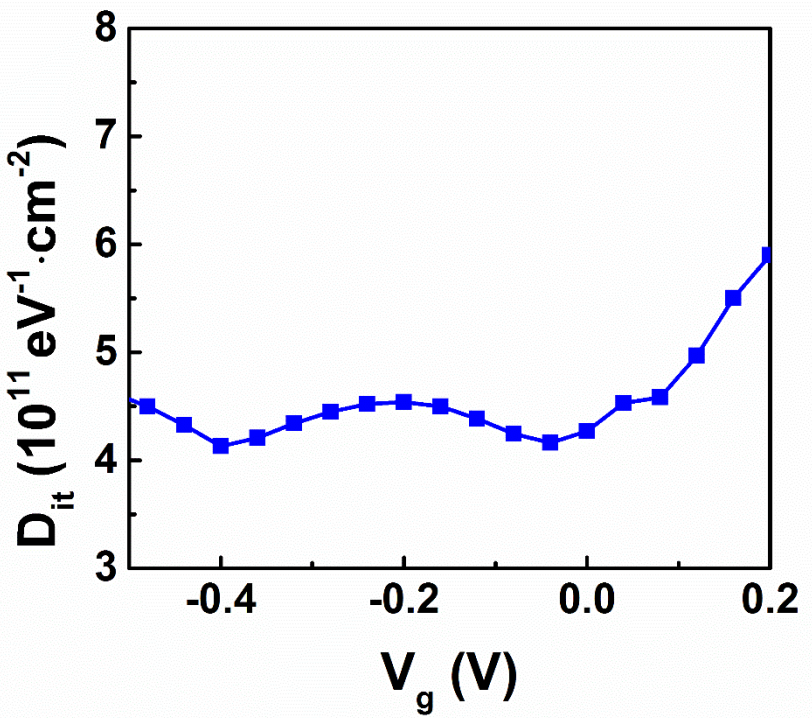
A simple process for sidewall CV characterization

MOS Sidewall

- **C-V characteristics**

Conductance method

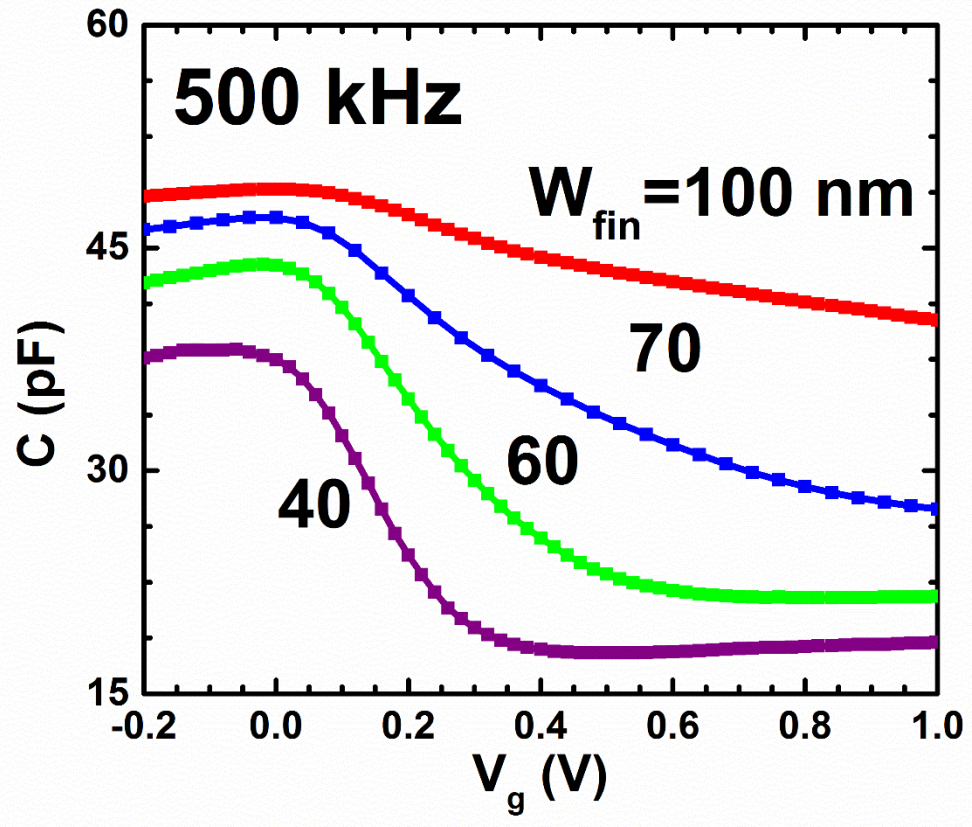




- $D_{it} \sim 5 \cdot 10^{11}$ $eV^{-1} \cdot cm^{-2}$ close to valence band edge
- Comparable to planar GaSb: $D_{it} = 3 \cdot 10^{11}$ $eV^{-1} \cdot cm^{-2}$ (Nainani, *TED*, 2012)

MOS Sidewall

- **Impact of fin width**

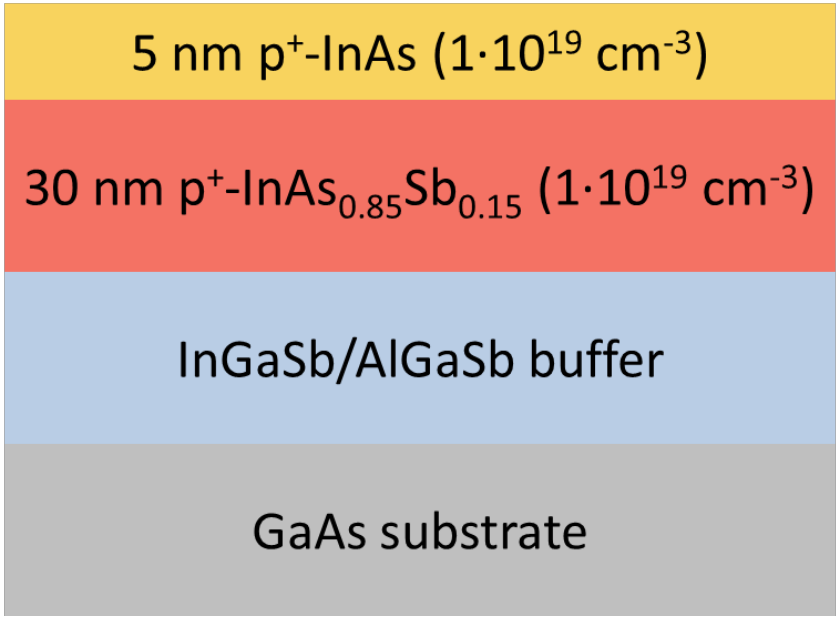


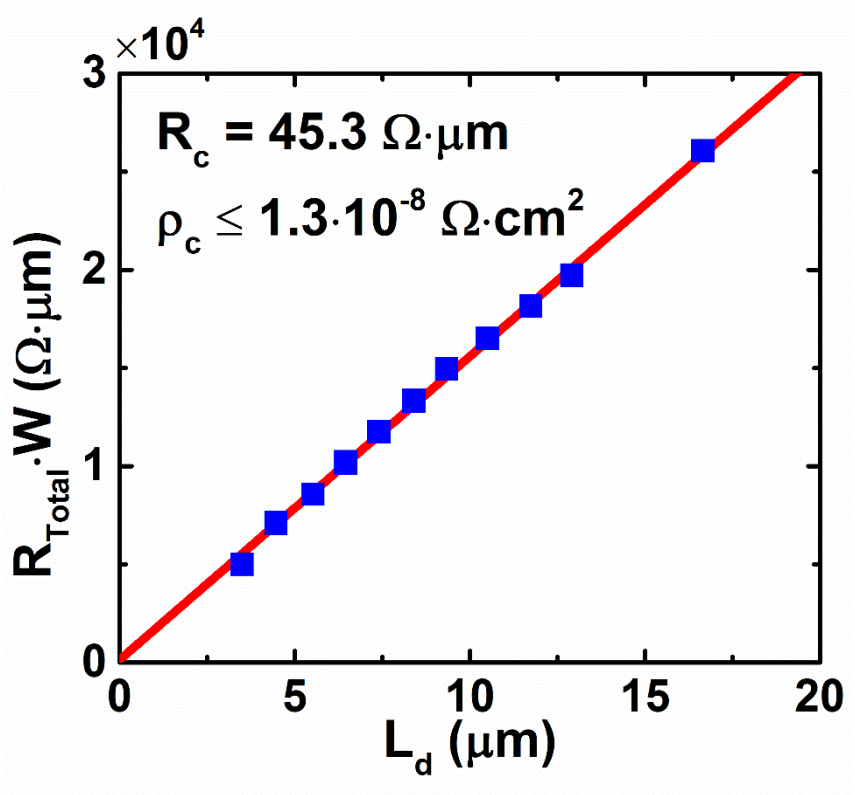
$W_f \downarrow \rightarrow$ Sharper CV

Ohmic Contacts

- **Ni/Pt/Au** contacts

Guo, *EDL*, 2015

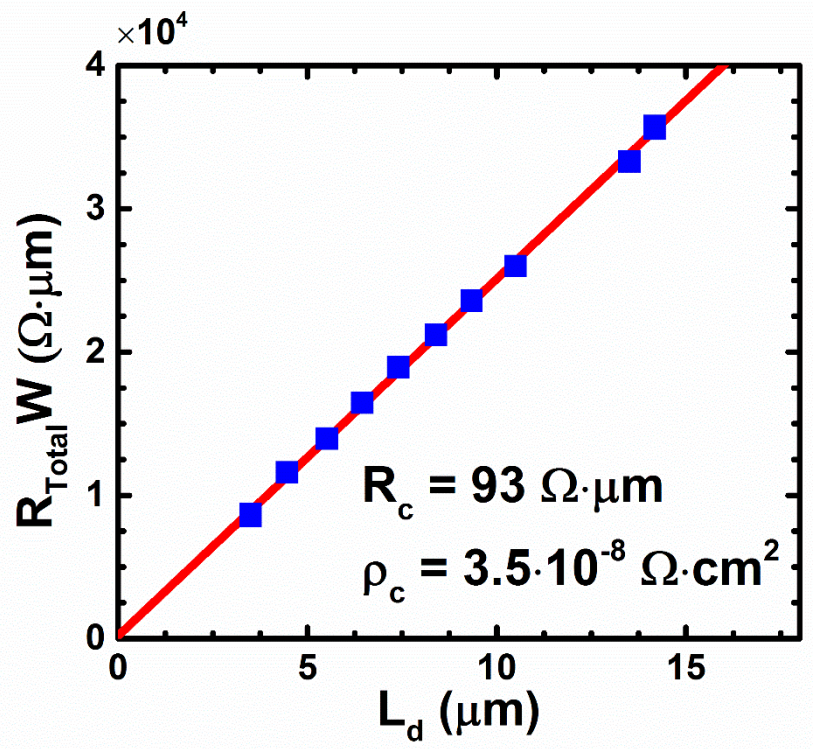


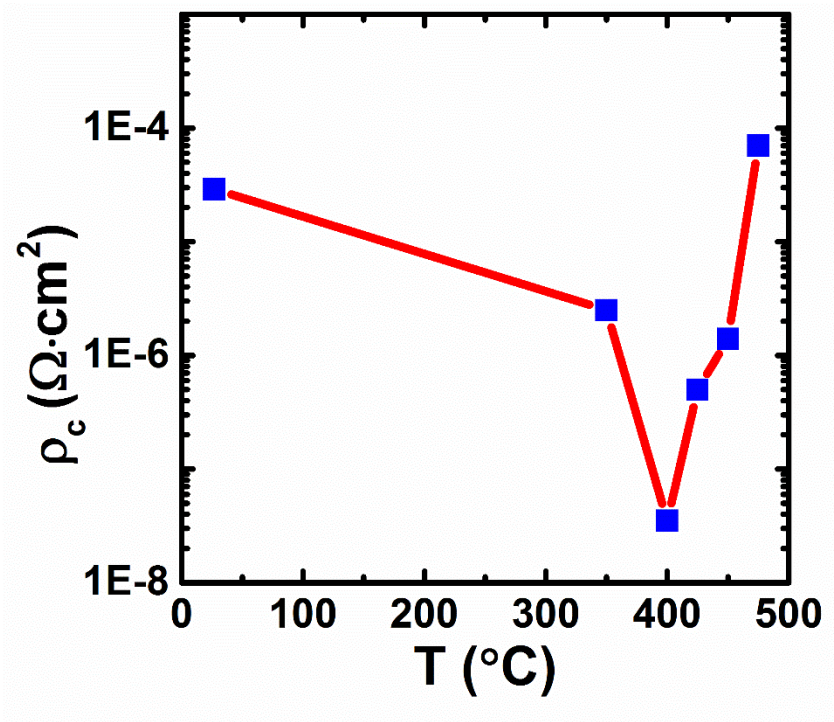


Au-containing contacts with ultra-low ρ_c

Ohmic Contacts

- **Ni/Ti/Pt/Al** contacts



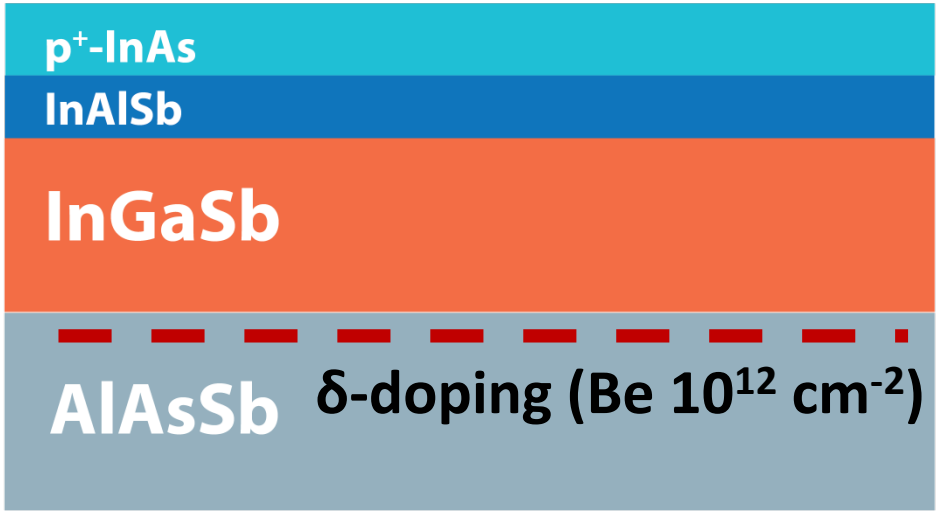


Si-compatible contacts with ultra-low ρ_c

InGaSb FinFET Process

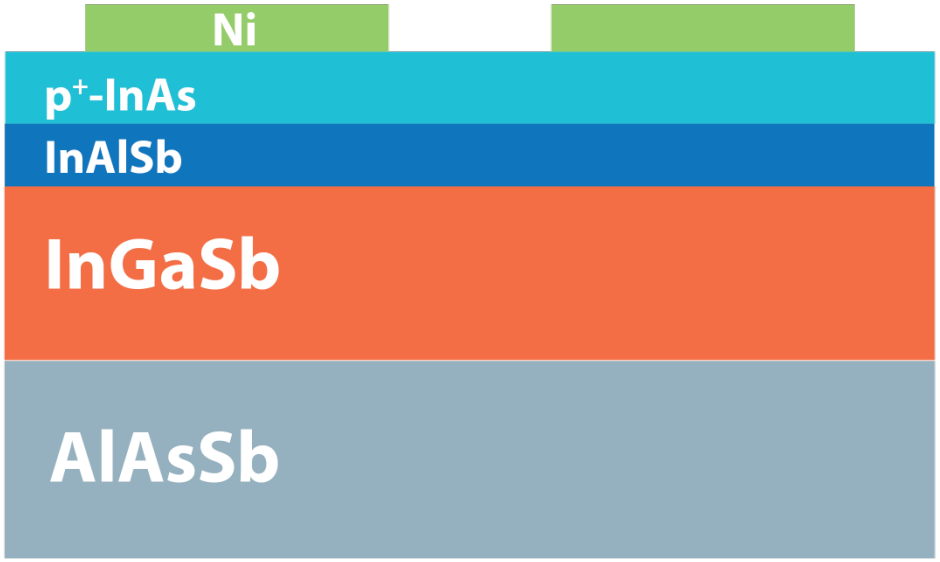
- **InGaSb channel compressively stressed (-2.3%)**

MBE by Sandia National Laboratory



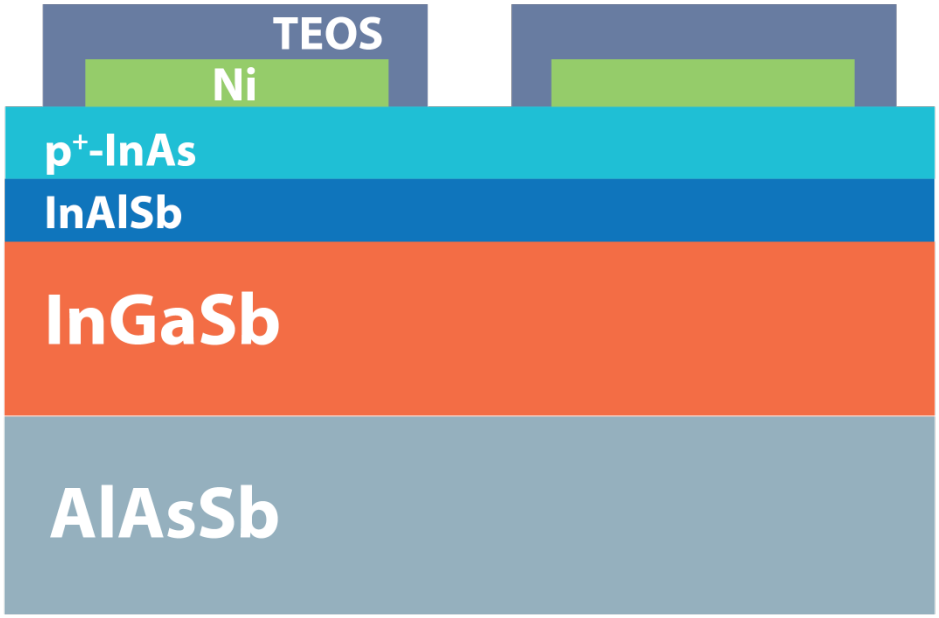
Starting heterostructure

InGaSb FinFET Process



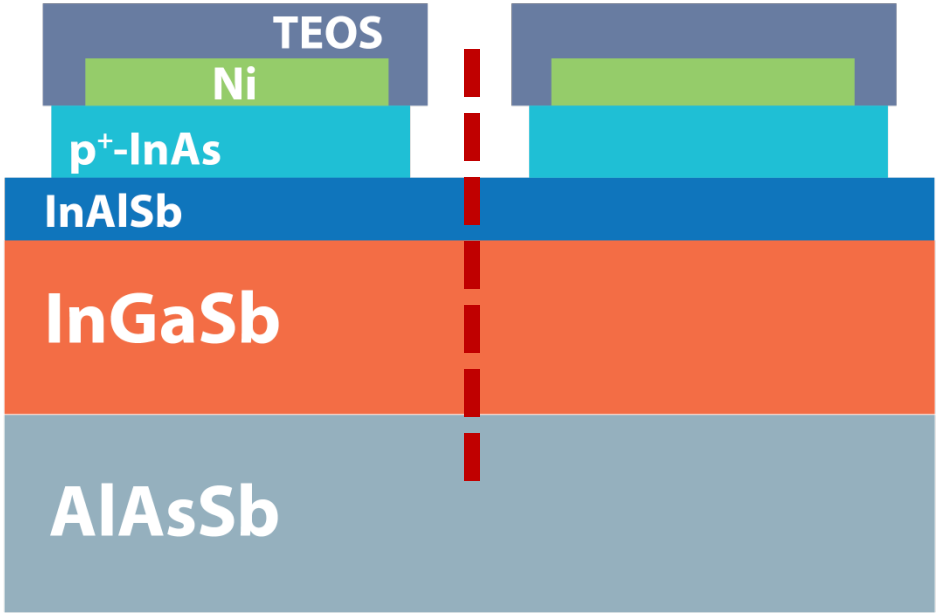
Ni ohmic contacts

InGaSb FinFET Process



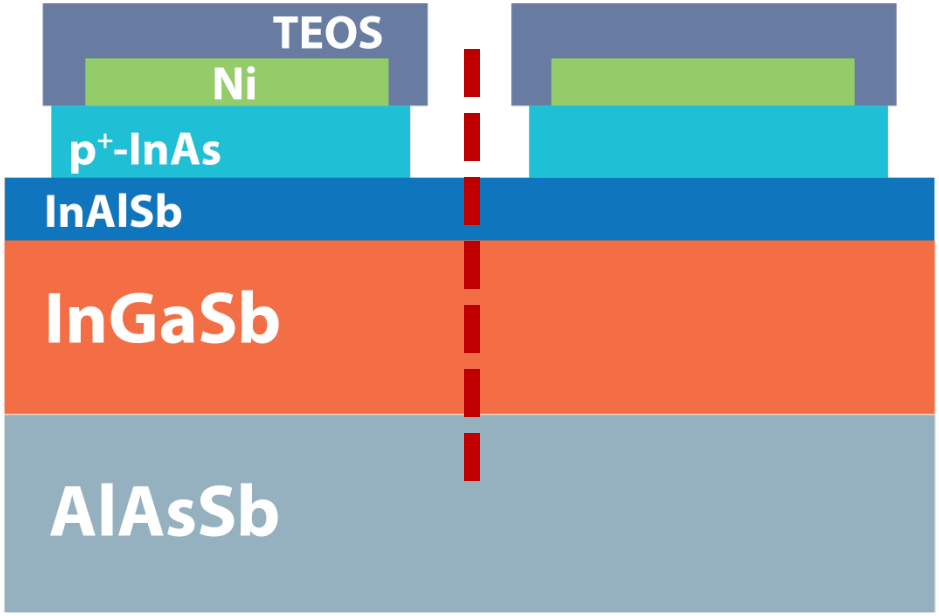
Gate + mesa

InGaSb FinFET Process



p^+ cap recess (wet)

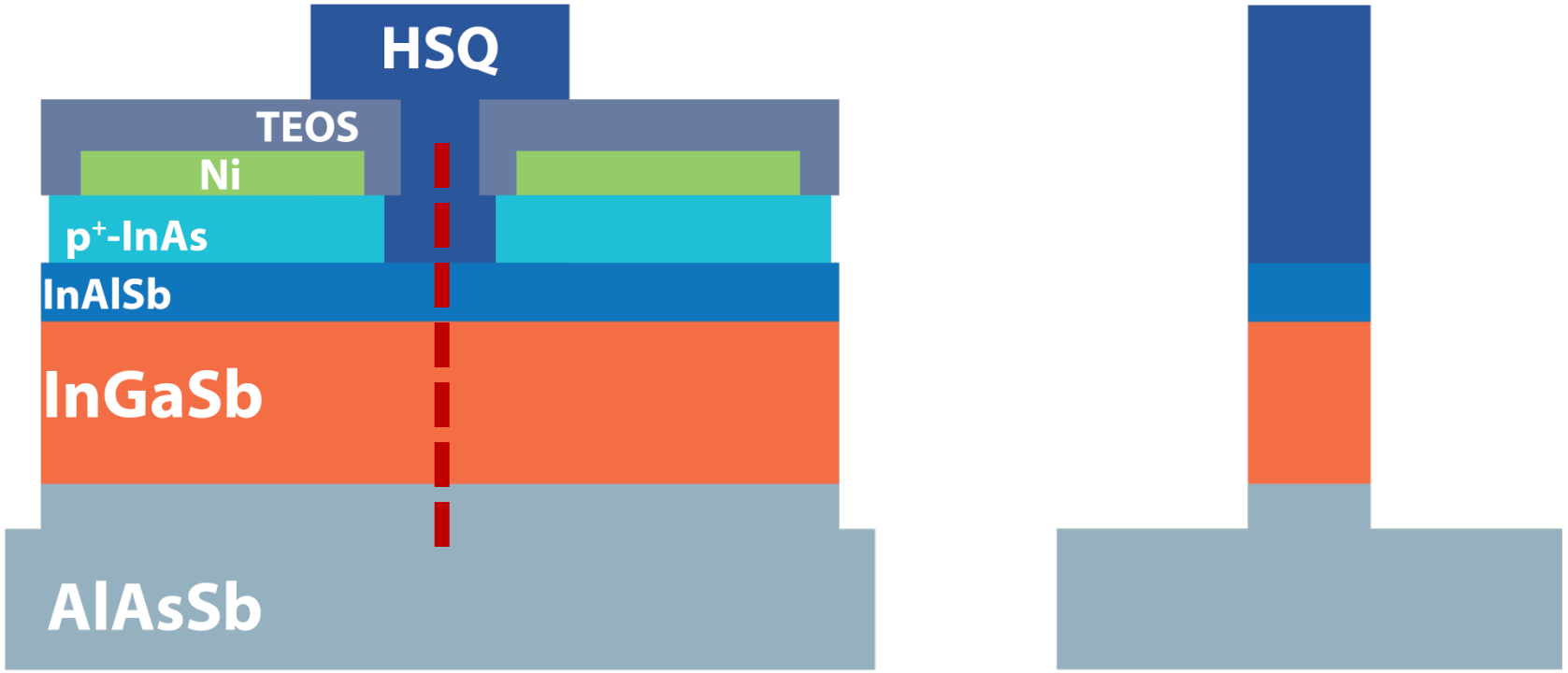
InGaSb FinFET Process



p^+ cap recess (wet)

InGaSb FinFET Process

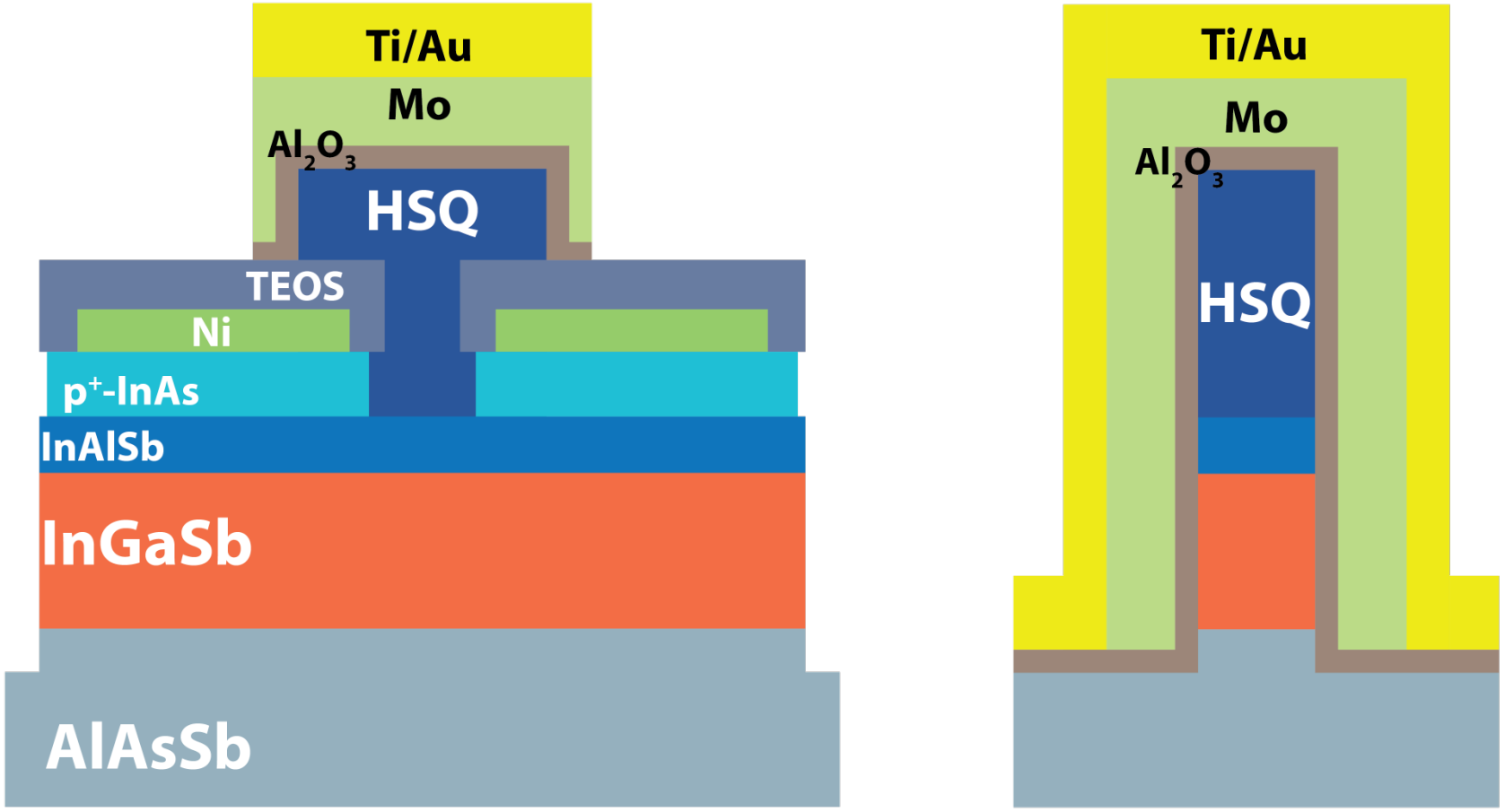
- **RIE by BCl_3/N_2 chemistry**
- **No sidewall treatment after etch**



Fin RIE (mesa)

InGaSb FinFET Process

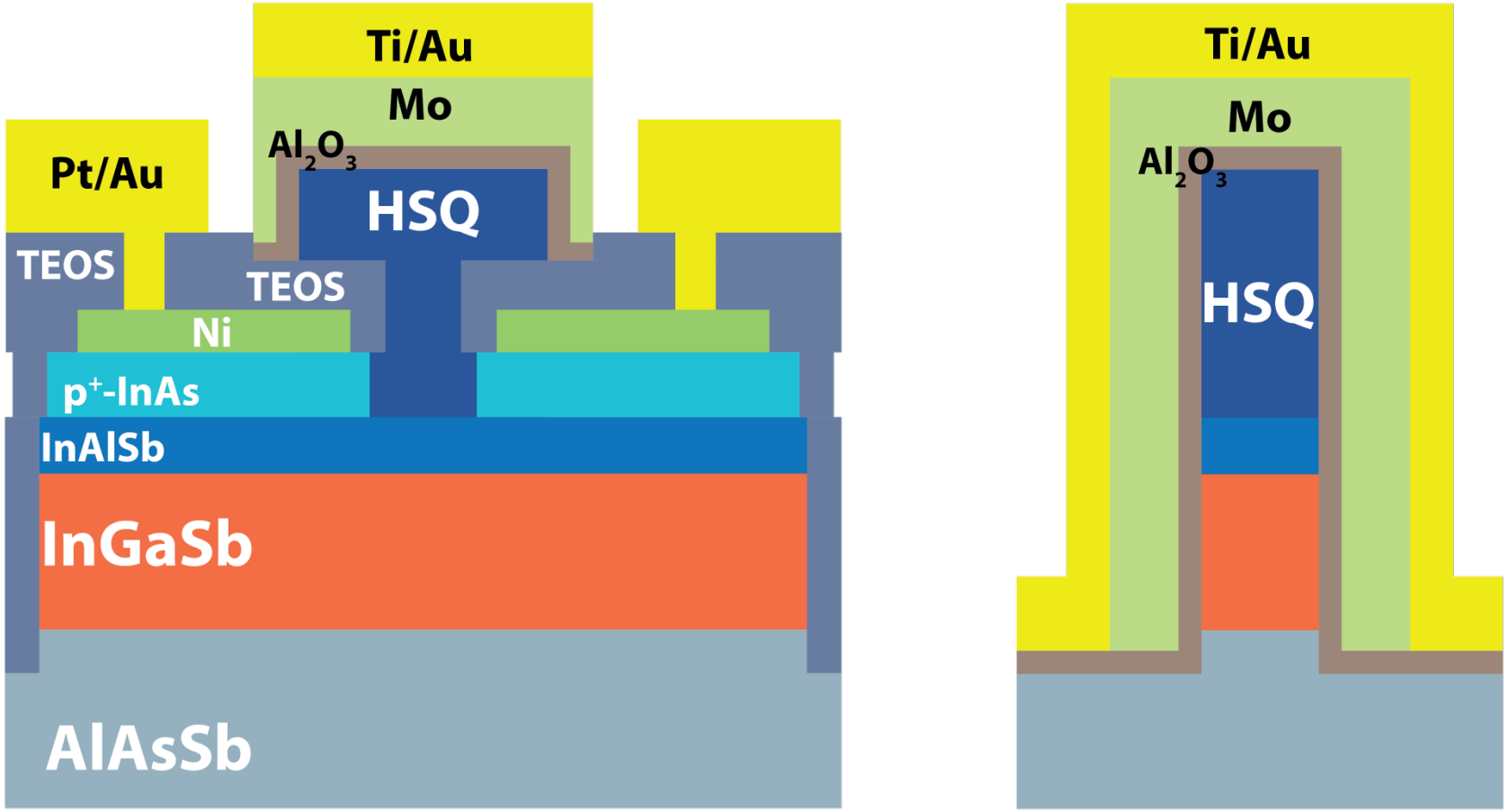
- 4 nm Al_2O_3 (EOT = 1.8 nm)



Gate ALD & metal

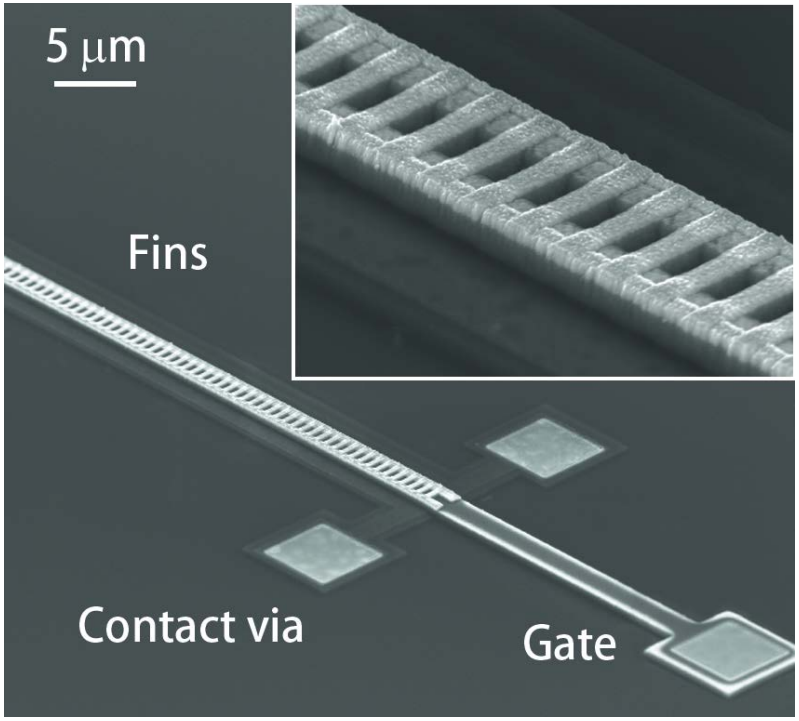
InGaSb FinFET Process

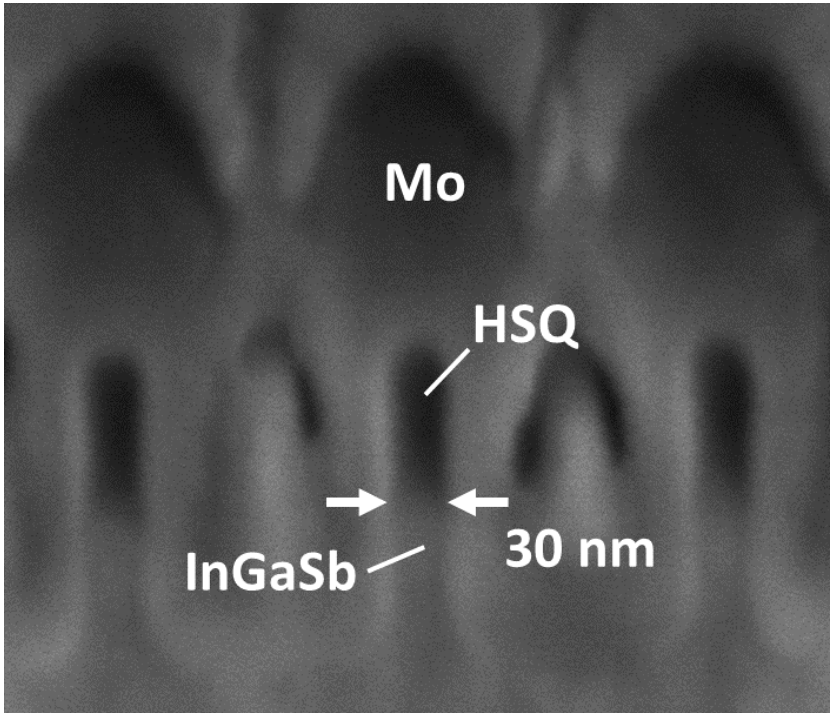
- **Double gate**



Via & pad deposition

InGaSb FinFETs
Finished Devices

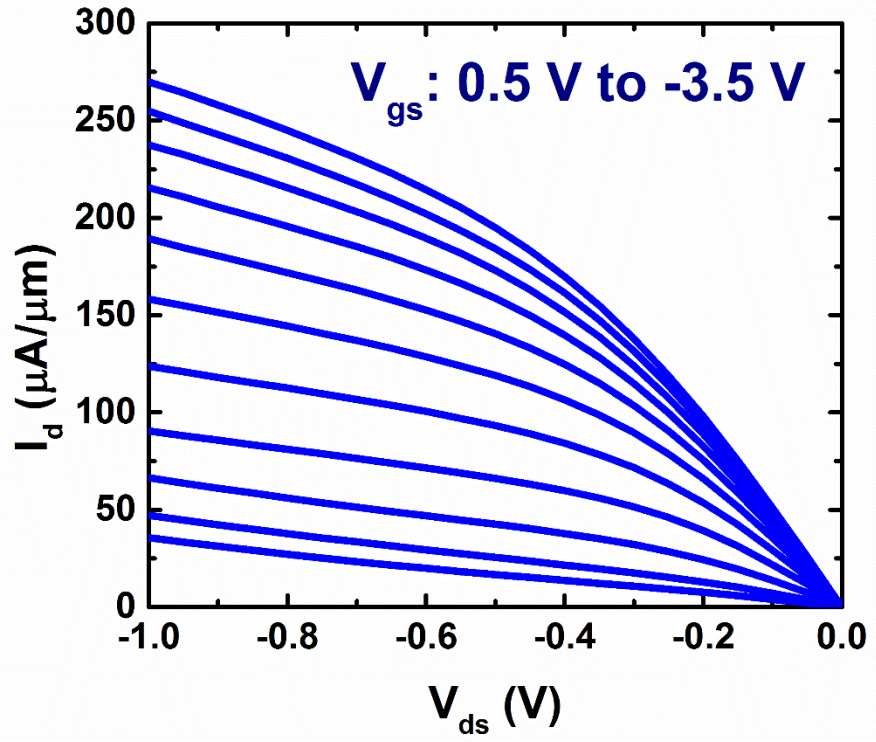


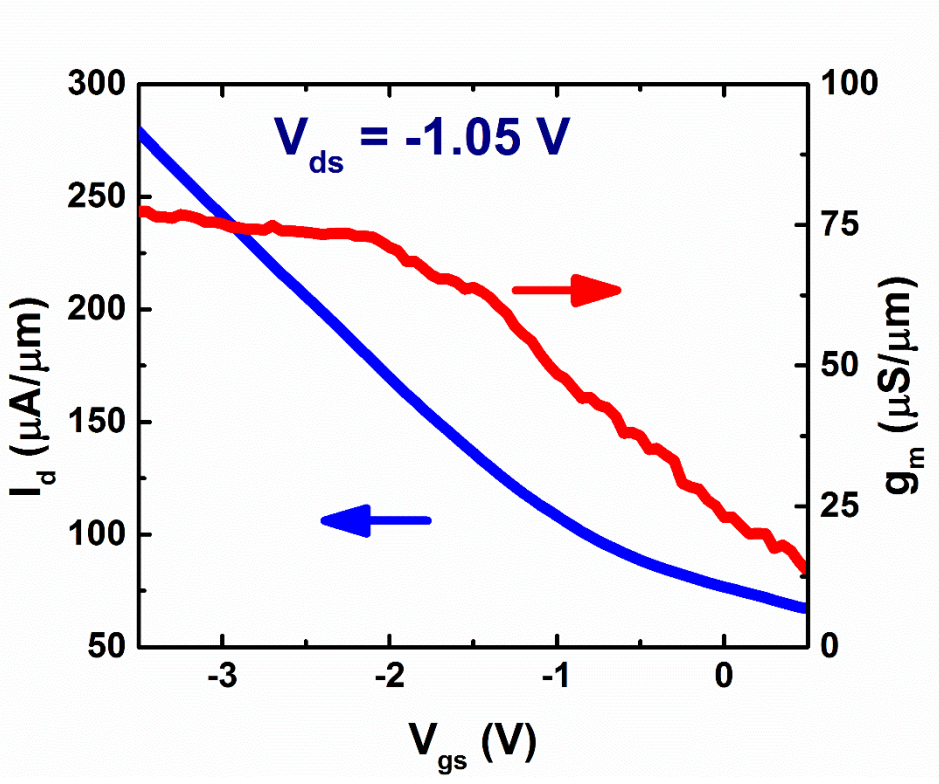


W_f = 30 – 100 nm, L_g = 0.1 – 1 μm, N_f = 70

Output & g_m Characteristics

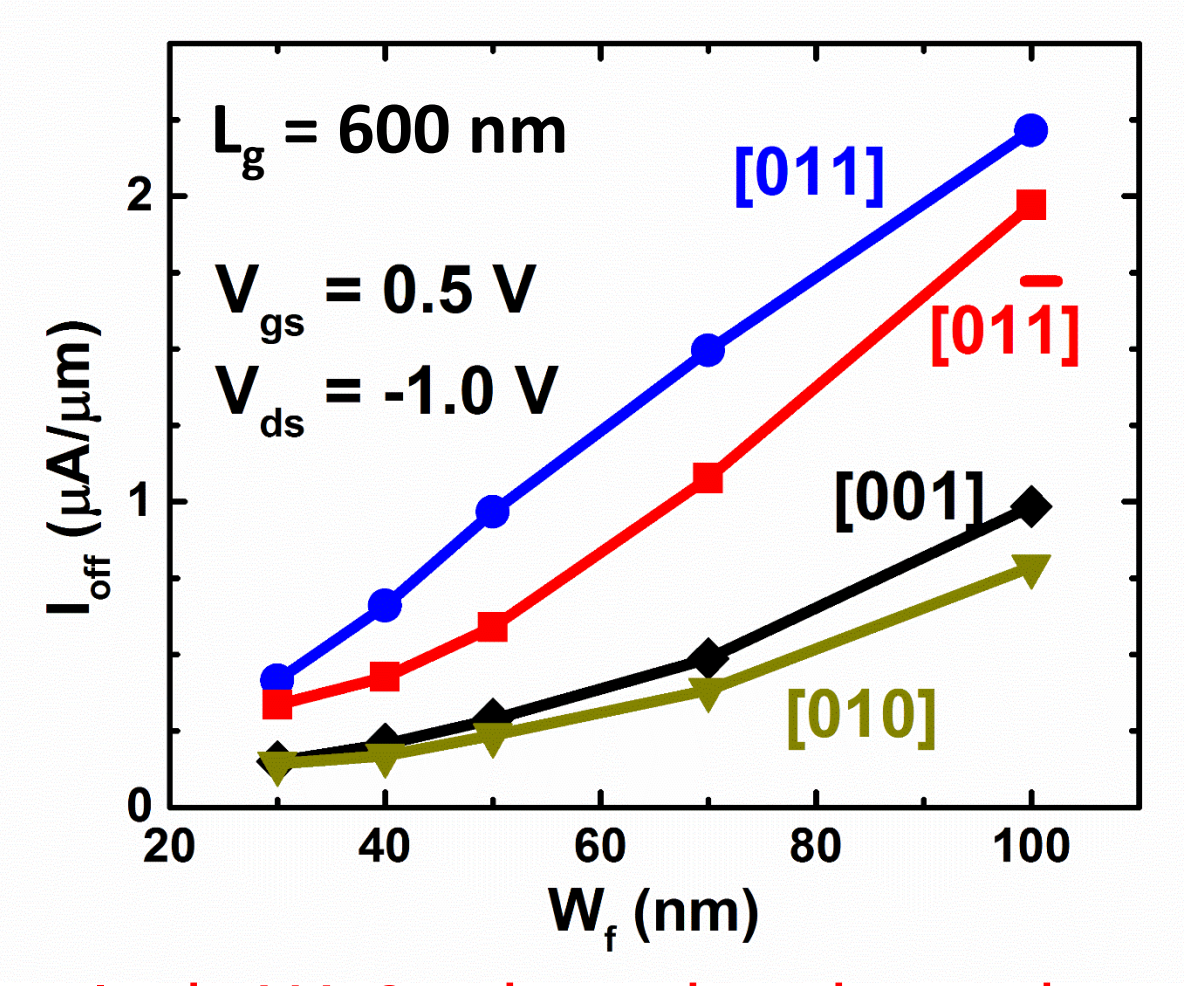
- W_f = 30 nm, L_g = 100 nm, EOT = 1.8 nm
- Normalized by $2N_fH_{ch}$





Suffer from poor turn-off

Off Current

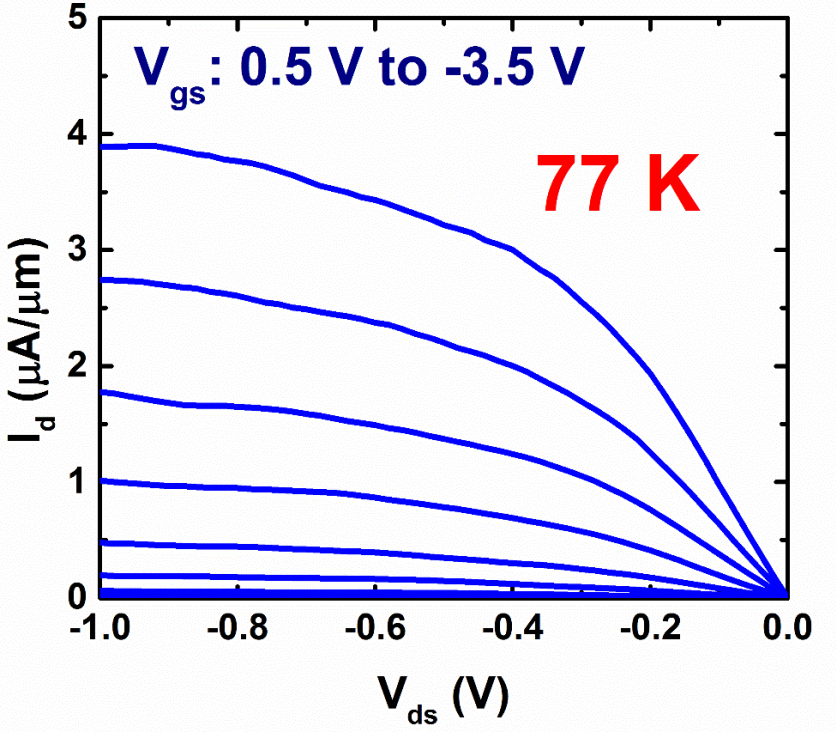


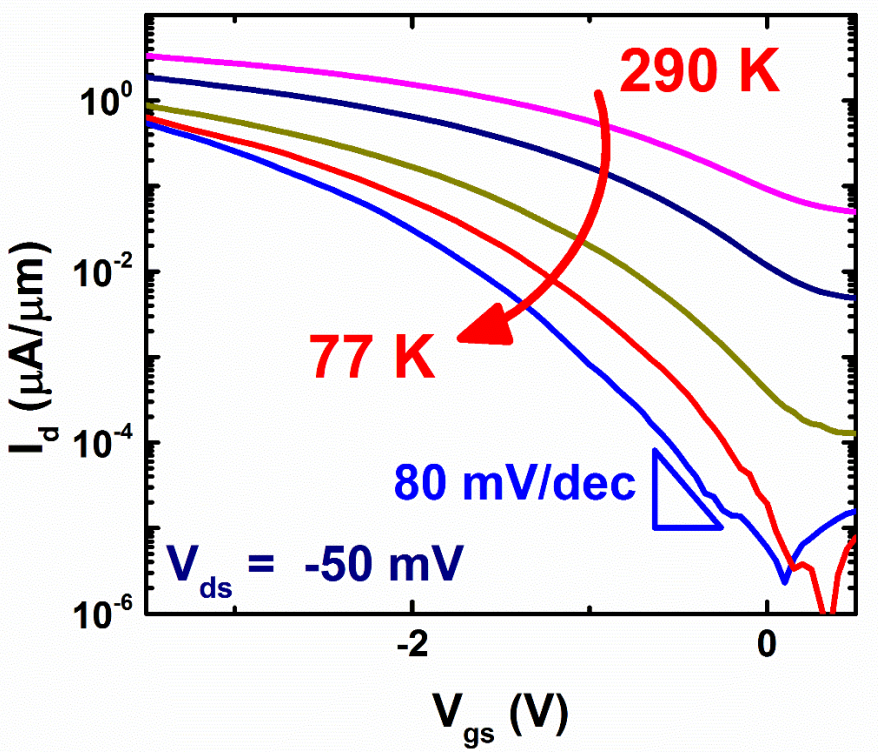
I_{off} is W_f & orientation dependent

→ Off-state leakage current flows inside fin

Low Temperature Characteristics

- W_f = 30 nm, L_g = 300 nm



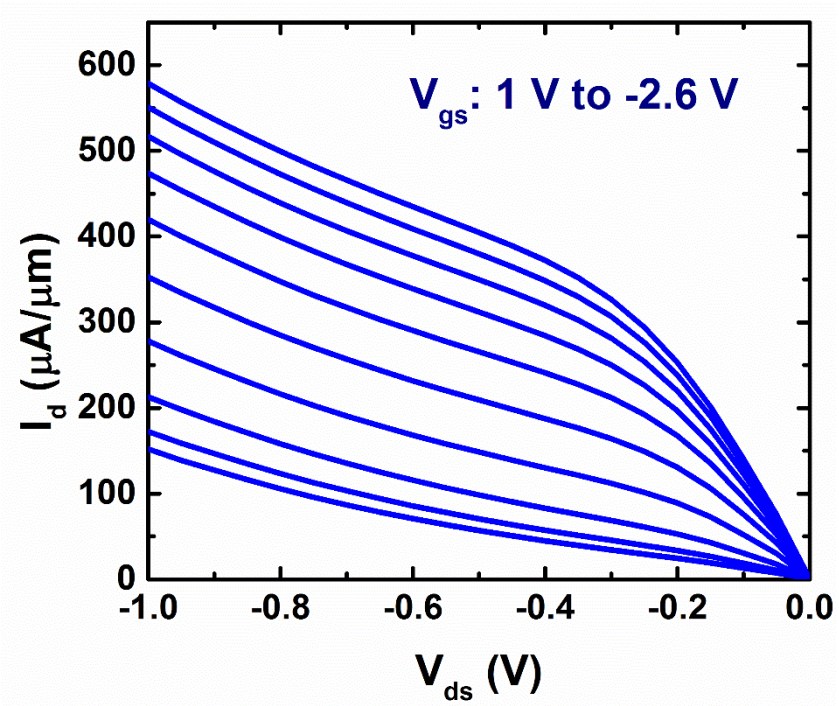


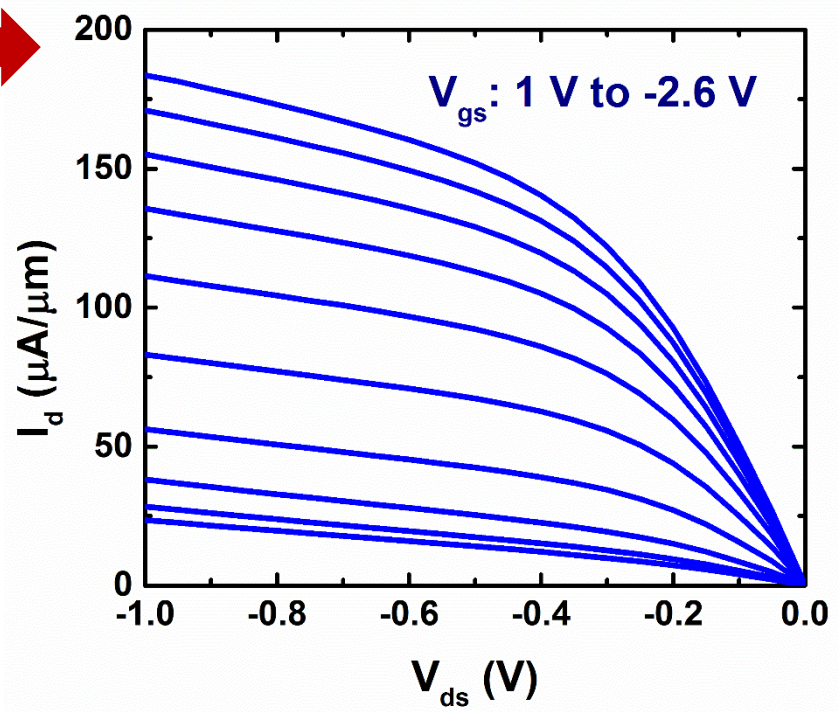
- Leakage mitigated at low temperature
- Leakage within the fin

Fin Sidewall Passivation

W_f = 70 nm, L_g = 250 nm

1% HCl 30s after fin RIE

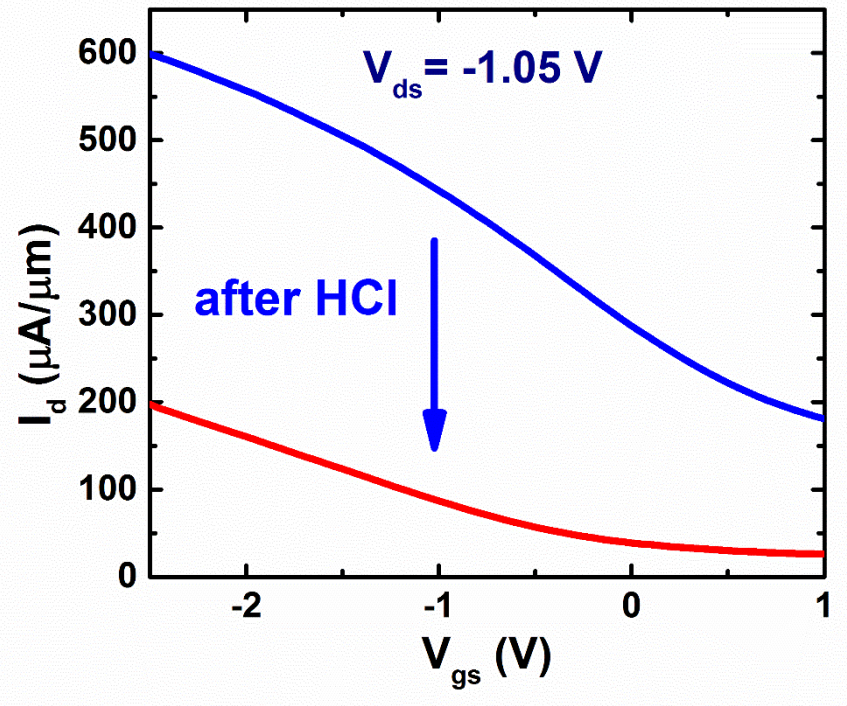




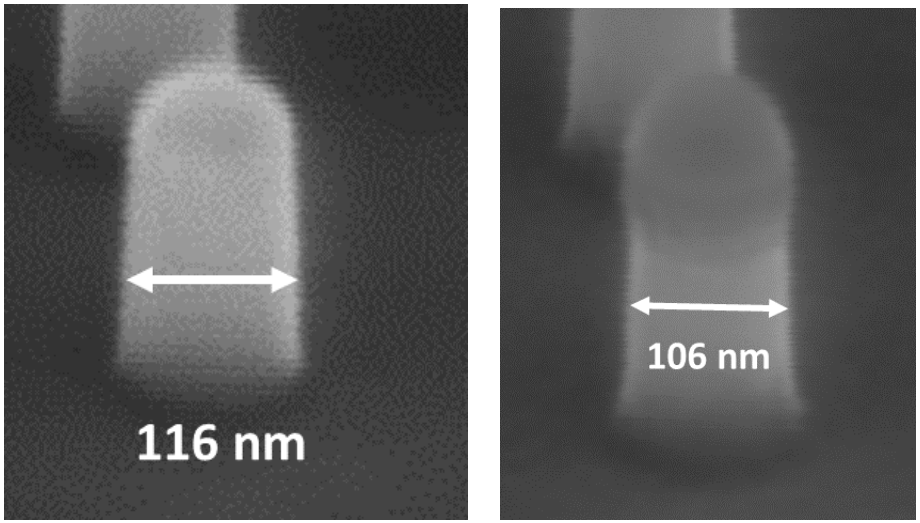
Improved turn-off

Fin Sidewall Passivation

- **1% HCl 30s after RIE**

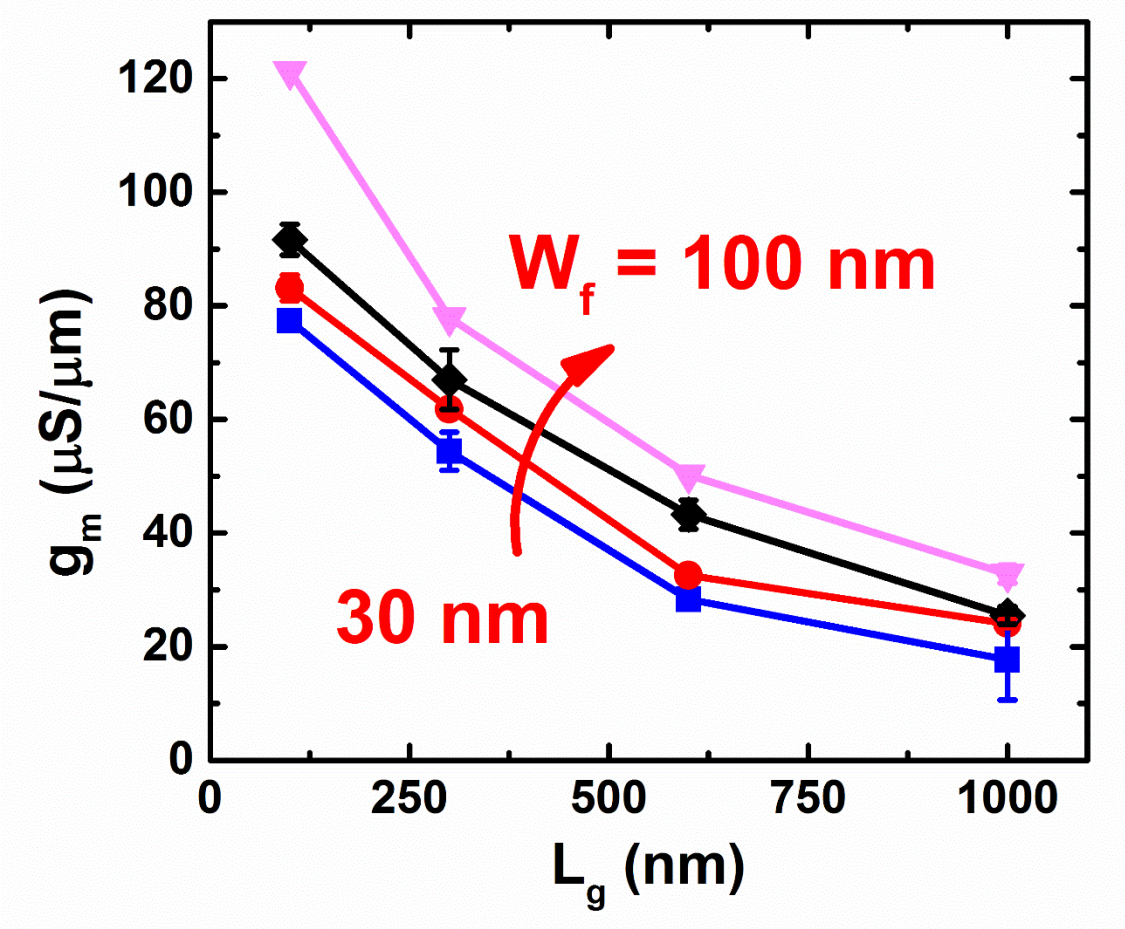


After HCl



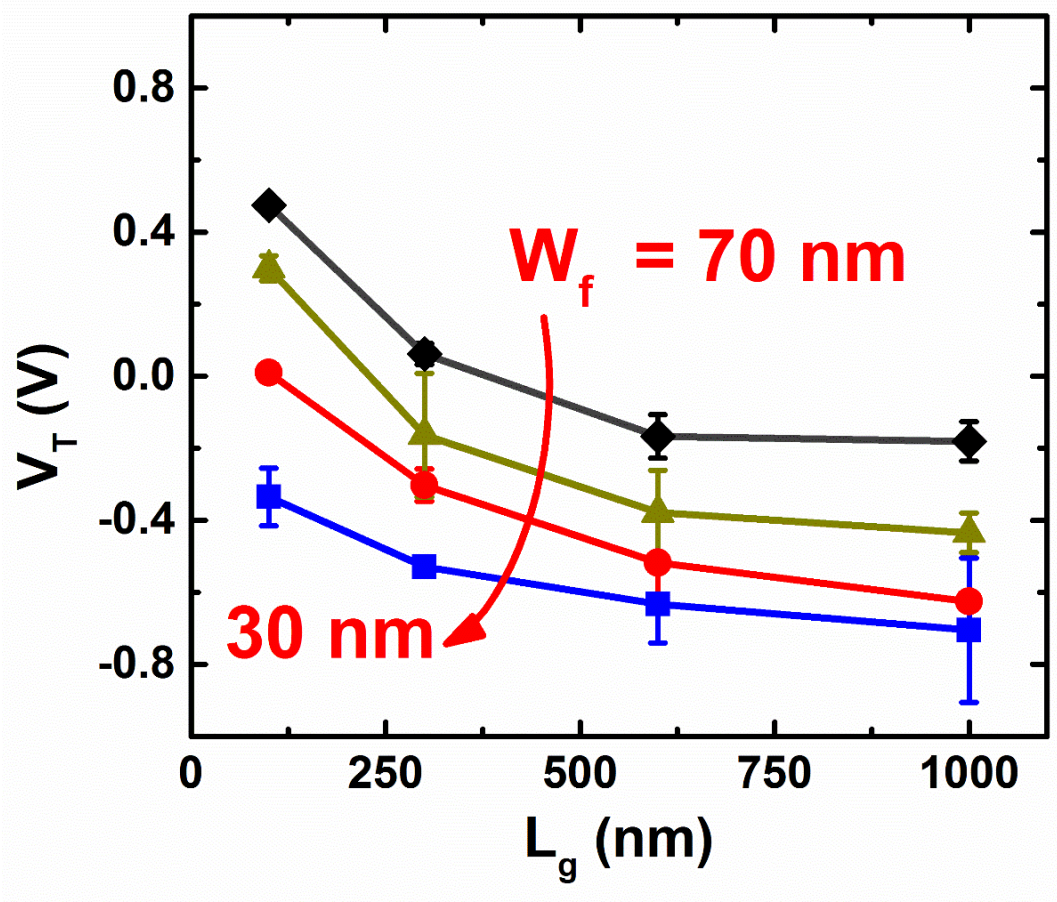
Need better fin passivation technology

g_m Scaling



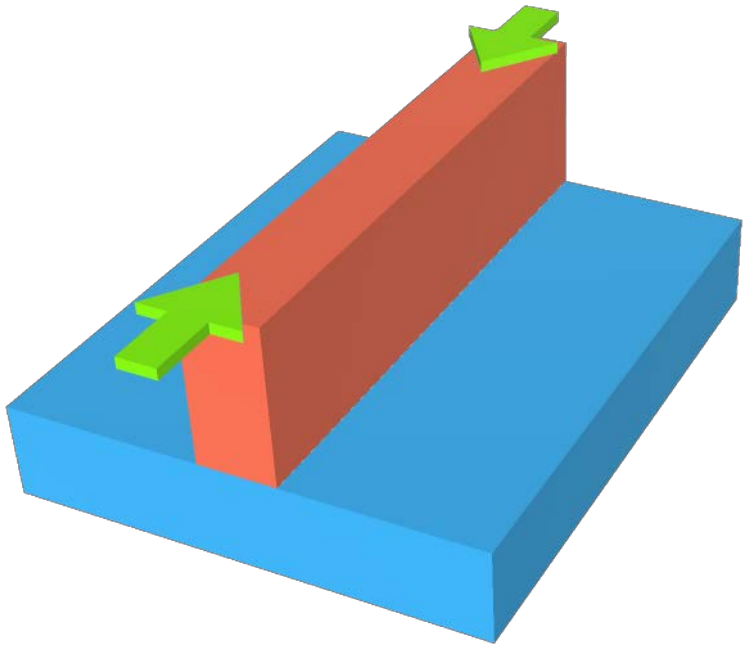
$W_f \uparrow$ or $L_g \downarrow \rightarrow g_m \uparrow$

V_T Scaling



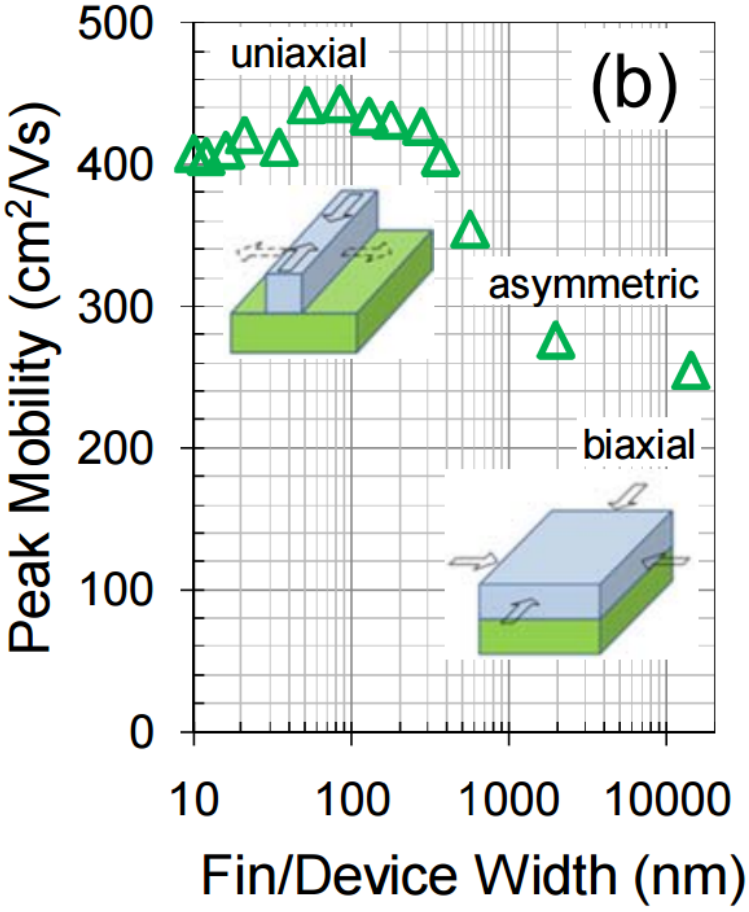
$W_f \downarrow \rightarrow \Delta V_T < 0$, improved V_T roll-off

Orientation Analysis



SiGe p-FinFET

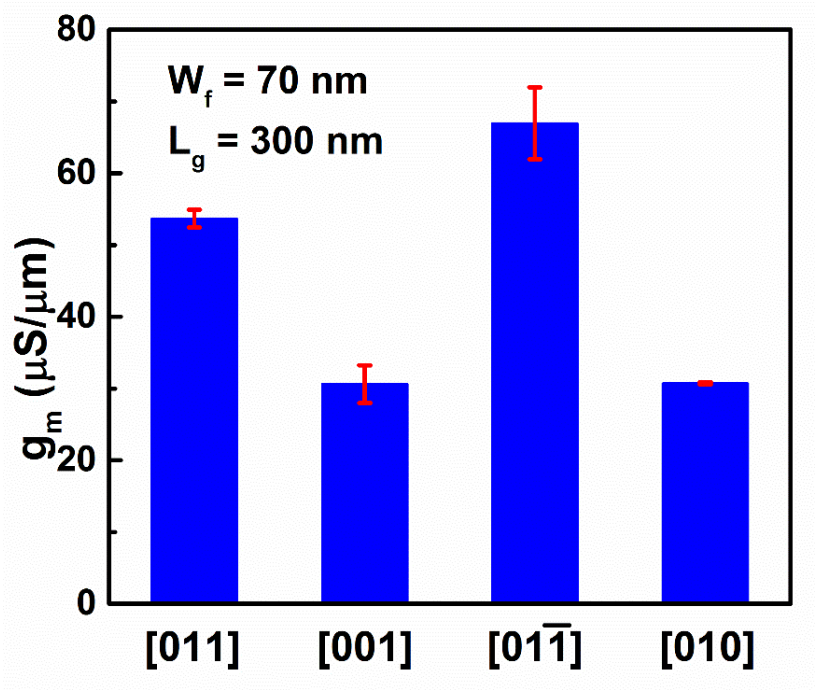
Hashemi, *IEDM*, 2014



- Uniaxial strain in fin
- Piezoelectric effect

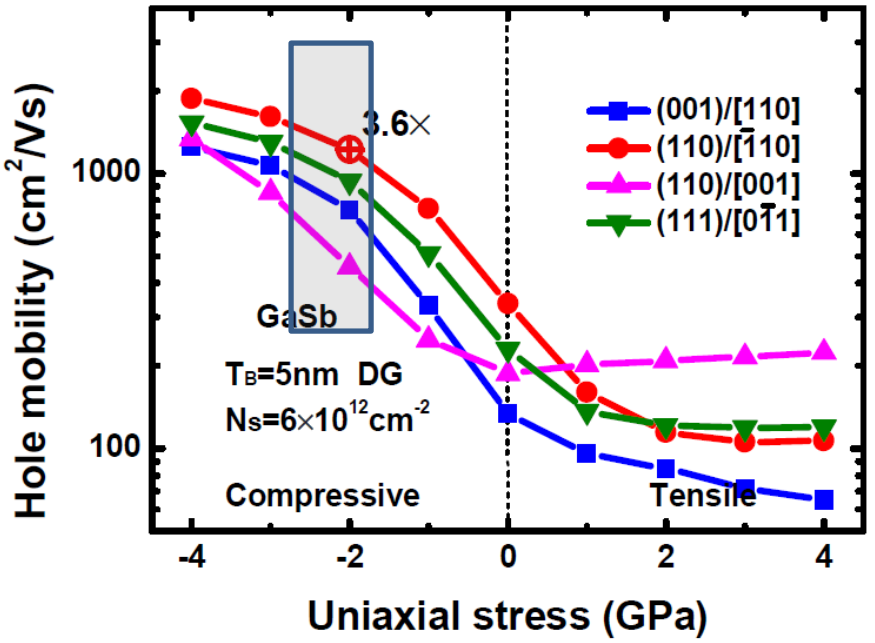
Orientation Analysis

InGaSb FinFET



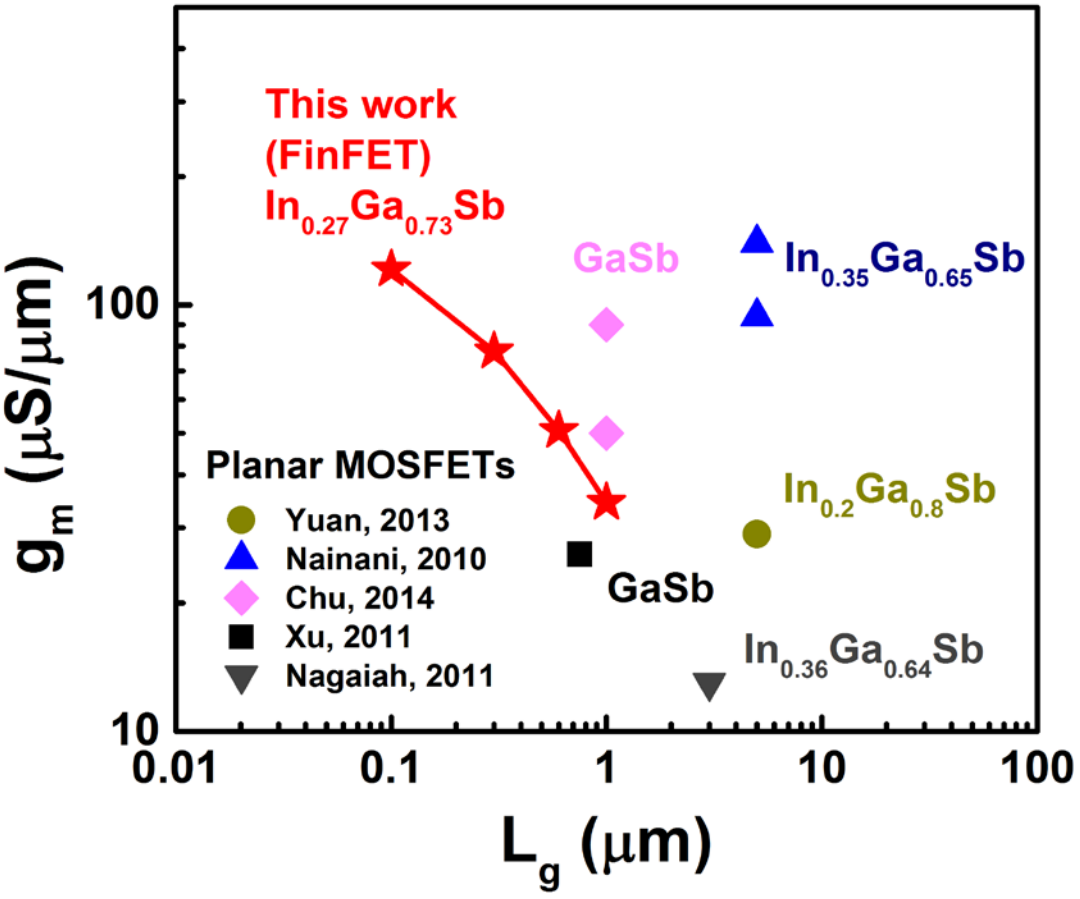
GaSb DG MOSFET (Sim.)

Chang, *IEDM*, 2014



g_m exhibits strong dependence on fin orientation

Benchmark: InGaSb MOSFET



- First InGaSb FinFET
- Peak g_m approaches best InGaSb planar MOSFETs

Conclusions

- **Developed new InGaSb FinFET technology**
  - Nanometer-scale fin RIE: $W_f \geq 15$ nm, AR > 10, fin angle > 85°
  - Double-gate sidewall capacitor with low D_{it}
  - Si-compatible ohmic contacts: $\rho_c = 3.5 \cdot 10^{-8}\ \Omega \cdot cm^2$
- **Demonstrated first InGaSb p-channel FinFET**
  - Performance comparable to best planar InGaSb MOSFETs

Thank You!